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SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING

Abstract

A method of formation of a deep trench vertical transistor is provided. A deep trench with a sidewall in a doped semiconductor substrate is formed. The semiconductor substrate includes a counterdoped drain region in the surface thereof and a channel alongside the sidewall. The drain region has a top level and a bottom level. A counterdoped source region is formed in the substrate juxtaposed with the sidewall below the channel. A gate oxide layer is formed on the sidewalls of the trench juxtaposed with a gate conductor. Perform the step of recessing the gate conductor below the bottom level of the drain region followed by performing angled ion implantation at an angle $\theta+\delta$ with respect to vertical of a counterdopant into the channel below the source region and performing angled ion implantation at an angle θ with respect to vertical of a dopant into the channel below the source

region